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Low Power FinFET Based Full Adder Design Using GDI Method

[1]Krithiga Sukumaran, [2]Janani Munisamy

[1]Assistant Professor, Department of ECE, ThanthaiPeriyar Government Institute of Technology (TPGIT) India
[2]Assistant Professor, Department of ECE, ThanthaiPeriyar Government Institute of Technology (TPGIT) India

E-mail: krithiga.sri@gmail.com, jananigms@gmail.com

Krithiga Sukumaran

Janani Munisamy

A B S T R A C T

The electronic market is growing very rapidly because most of the devices are compact, innovative, an efficient and consume less power. Because of the advancement in the semiconductor technology, integration of the whole electronics system on a single chip is practicable. Conventional CMOS has a Short Channel Effect. To reduce the Short Channel Effect, FinFET is used. FinFETs are the new emerging transistors that can work in the nanometer range to overcome these Short Channel Effects. Gate Diffusion Input (GDI) is used to reduce the power consumption of digital circuits. FinFET based digital circuits such as full adder is designed by using the GDI technique. The short gate mode is used here (SG). The technology node used is 20nm at HSPICE Software.

Keywords: FinFET, Full adder, GDI, Short Channel Effect.

1. INTRODUCTION

Due to the development of technology, is essential to have a chip that requires minimum power, less power delay with efficient output. The improved digital circuits are designed in terms of less number of transistors, delay, average power, power delay product. Short channel effects occur in MOSFETs in which the channel length is comparable to the depletion layer widths of the source and drain junctions. These effects include, in particular drain-induced barrier lowering, velocity saturation, and hot carrier degradation. In order to reduce the Short Channel Effects, and power consumption FinFET based GDI digital circuit is designed.Here 20nm Technology node is used.

The GDI (gate diffusion input) technique is using FinFET. This technique has its advantages. The full adder is one of the basic blocks of in many digital circuits like FPGA and ALU. Hence it is designed with less number of transistors and less delay compare with the conventional combinational circuits.

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Moore's Law refers to Moore's perception that the number of transistors on a microchip doubles every two years, though the cost of computer is halved. Due to the increase of complexity on a chip the area and power consumption of the chip gets increases. As the power consumption increases, the temperature on the device increases which further changes the characteristics of the device. FinFET technology provides the high drive current for a given transistor footprint, Hence high speed, low leakage current, hence low power consumption. The GDI method [1] allows reducing power consumption, propagation delay, and area of the digital circuit.

FinFET (Fin shaped FET) is a type of field effect transistor (FET) that has a thin vertical fin type structure. A FinFET is fabricated in a silicon layer overlying an insulating layer with the device extending from insulating layer as a fin. To provide enhanced drive current and effectively suppressed short channel effects, double gates are provided over the sides of the channel in FinFET.

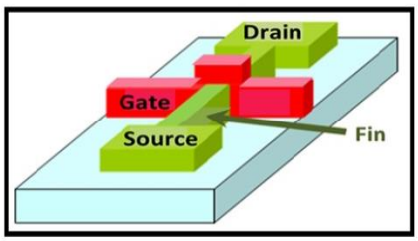

Fig.1 Double gate FinFET

FinFET technology provides numerous advantages over bulk CMOS, such as higher drive current for a given transistor footprint, hence higher speed, lower leakage, hence lower power consumption.

1.1 MODES OF OPERATION

There are 4 types of operation modes in FinFET [2]. They are,

- Short gate (SG) mode
- Independent gate (IG) mode
- Low power (LP) mode
- IG/LP mode.

1.1.1 The Short-gate (SG) mode

In this mode of operation both p-type FinFET and n-type FinFET back gate are short circuited to its front gateand has only one terminal.The three terminals are Gate,Source and Drain.There is no external control of the threshold voltage. Fig.2 shows NAND gate using shorted gate mode. This configuration is best suitable for high performance applications.

Advantages

- Fastest under all load conditions

1.1.2 The Independent gate (IG) mode

In this mode of operation the two gates are electrically independent, one to control the threshold voltage and the other gate for switching. It provides two different active mode of operation with significantly different current characteristics determined by the bias conditions, the NAND gate schematic in IG mode shown in Fig.3

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Advantages

- Very low leakage
- Low switched capacitance

1.1.3 The Low power (LP) mode

In this mode back-gate is tied to a reverse-bias voltage to reduce sub-threshold leakage, leakage power and the drive strength of every FinFET. A low voltage to n-type FinFET and high voltage to p-type FinFET is applied. This varies the threshold voltage of the devices, which reduces the leakage power dissipation at the cost of increased delay the NAND gate in LP mode is shown in Fig.4

Advantages

- Low area and switched capacitance.

1.1.4 The hybrid (IG/LP) mode

This mode is a combination of LP and IG modes and the delay is balanced by reducing the strength of the NAND gate schematic for hybrid mode is shown in Fig.5

Advantages

- Low leakage
- Low Area and switched capacitance

For example, NAND gate schematic diagram for all 4 different modes is given below.

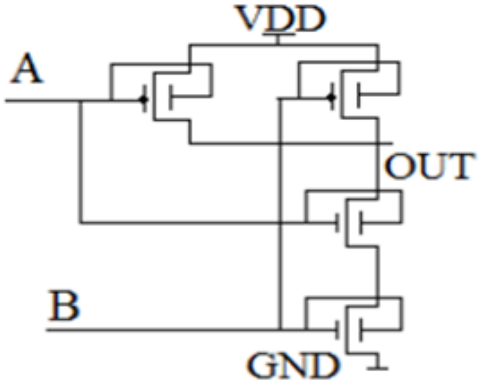

Fig.2 SG mode NAND gate

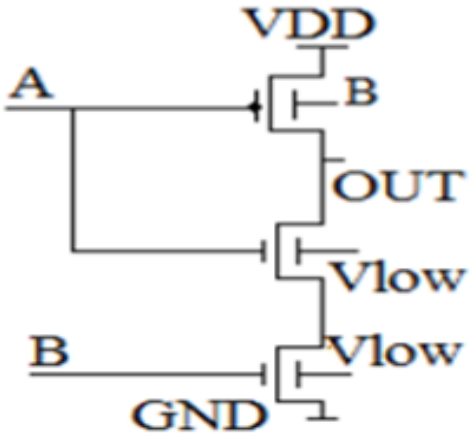

Fig.3 IG mode NAND gate

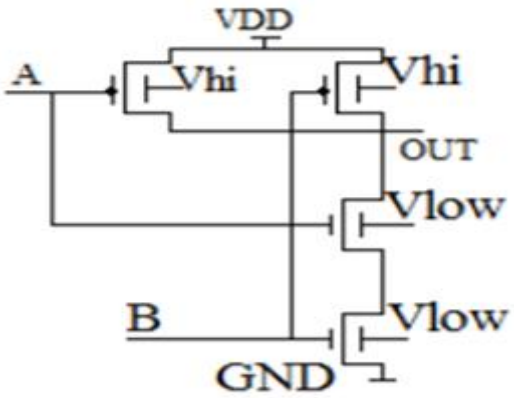

Fig.4 LP mode NAND gate

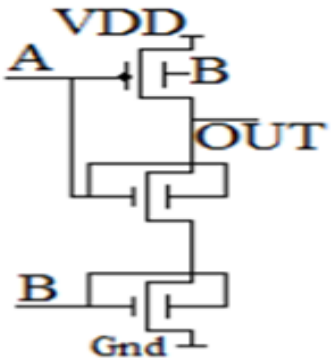

Fig.5 Hybrid (LP/IG) mode

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In this paper using Short Gate (SG) mode to design a digital circuits in FinFET. Because it provide faster operation and work under all load conditions.

1.2 GDI TECHNIQUE

Gate diffusion input is a new technique of low power digital combinatorial circuit design. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of the logic design.

At first glance, the basic cell reminds one of the standard CMOS inverters, but there are some important differences.

1. The GDI cell contains three inputs: G (Common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).

2. Bulk of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

The GDI cell structure is different from the existing techniques. It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies.

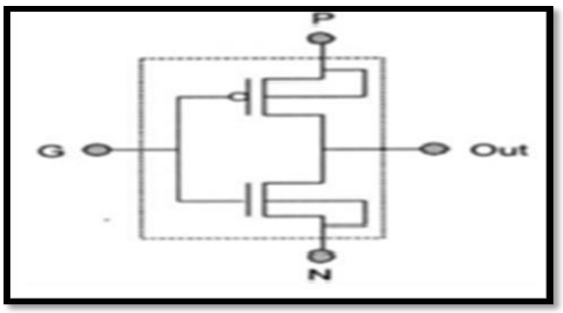

Fig.6 Basic GDI Cell

A GDI cell with four ports will be recognized as replacement multi-functional device, which may attain six functions with simply different combinations of input G, P and N

Table 1 Various Logic Functions of GDI cell for different Input configuration

N	P	G	OUT	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

Table 2 shows the comparison between GDI and the static CMOS design in terms of transistors count. It can be seen from table 2 that using GDItechnique AND, OR, Function 1, Function 2, XOR, XNOR can be implemented more efficiently. Function 1 and Function 2 are universal set for GDI, and consists of only two transistors, compared to NAND and NOR.These functions can be used synthesize other functions more effectively than NAND and NOR gates.

Table 2 shows the comparison between GDI and the static CMOS

FUNCTION	GDI	CMOS
INVERTER	2	2
F1	2	6
F2	2	6
OR	2	6
AND	2	6
MUX	2	12
XOR	4	16
XNOR	4	16
NAND	4	4
NOR	4	4

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2. WORKING OF FULL ADDER

A basic 1-bit full adder has three 1-bit inputs (A, B and C) and two 1-bit outputs (Sum and Carry). The output equations for the Sum and Carry are given as follows:

Sum = A xor B xor C … (1)

Cout = (A(A xnor B)) + (Cin(A xor B)) = (B(Axnor B)) + (Cin(A xor B)) … (2)

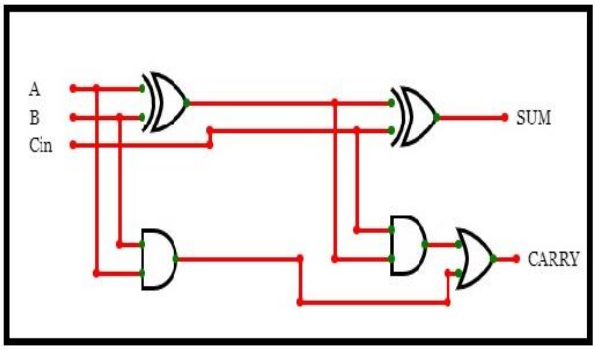

Fig.7 Logic diagram for Full adder

Table 3 Truth Table for Full adder

INPUT			OUTPUT	
A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum and Carry are implemented through the conventional CMOS full adder using 28 transistors [3]. Which consists of a PMOS pull-up and an NMOS pull-down network. The major drawback of that architecture includes the use of a large number of transistors, increasing the chip area. As a result, the propagation delay is relatively high.

2.1 PROPOSED DESIGN

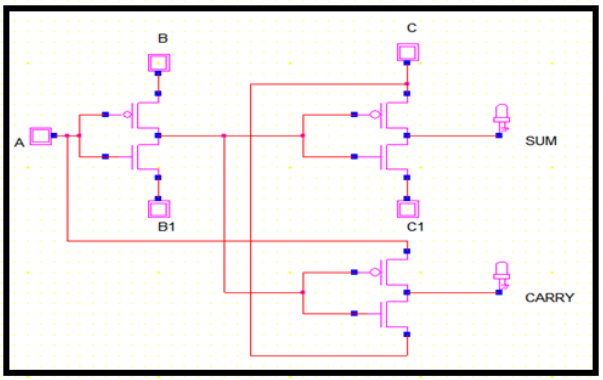

Fig.8 Proposed Full Adder circuit

This proposed GDI based full adder circuit consists of only 6 transistors. When compared to the previously proposed 10T full adder [4], the number of transistors is reduced by 4. The proposed full adder circuit is designed by combining two xor gates and one multiplexer. The inputs are A, B, B1, C, and C1, here B1 is the complement of B and C1 is the complement of C. The outputs are the sum and carry. The output of the sum is carried by two xor gates.

Sum= A xor B xor C …(3)

The output of Carry is carried by 2:1 multiplexer as,

Carry = ($\overline{A \oplus B}$) A. ($A \oplus B$) …(4)

3. DIFFERENT PARAMETERS

3.1.1 DYNAMIC POWER

Dynamic power is the power that is consumed by a device when it is actively switching from one state to another. Dynamic power consists of switching power consumed while charging and discharging the loads on a device, and internal power (also referred to as short circuit power), consumed internal to the device while it is changing state.

$P_D = C_L V 2_{DD} f_p$ … (5)

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3.1.2 STATIC POWER

Static power is the power consumed while there is no circuit activity. For example, the power consumed by a D flip-flop when neither the clock nor the D input has active inputs (i.e., all inputs are "static" because they are at fixed dc levels). Dynamic power is the power consumed while the inputs are active.

$P_S = I_{leakage} * V_{DD}$… (6)

Where P_S=Static power

$I_{leakage}$= Leakage current

3.1.3 DELAY

Delay in VLSI is time between trigger (change any signal level) on any pin or net of interest and the change in signal level of the same or other pin or net.

Rise time is the time during transition, when output switches from 10% to 90% of the maximum value. Fall time is the time during transition, when output switches from 90% to 10% of the maximum value.

Delay (τ) = T (rf) + T (fr)/2 … (7)

Where T (rf) = time for rising to falling

T (fr) = time for falling to rising

3.1.4 LEAKAGE POWER

Leakage Power is defined as an undesirable sub-threshold current in the channel of a transistor when the transistor is turned off.

$P=ACV^2 F_{CLK}$ … (8)

Where P is the power consumed,
A is the activity factor, i.e., the fraction of the circuit that is switching,
C is the switched capacitance,
V is the supply voltage,
and F is the clock frequency.

4. SIMULATION RESULT

HSPICE is one of the most detailed simulation tools. It can use complex transistor models and solve the differential equations to predict currents and voltages.

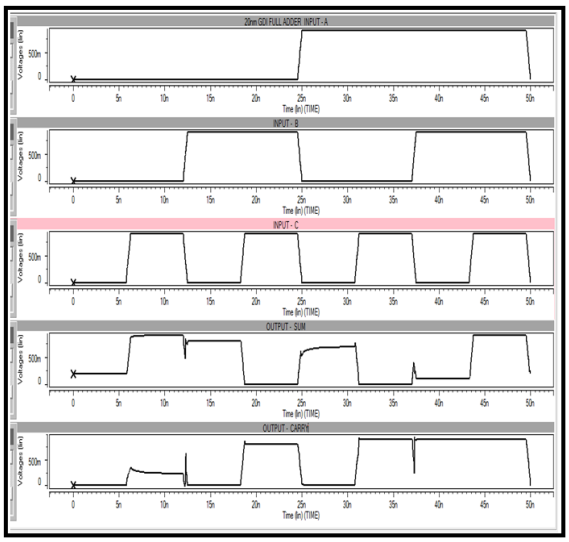

Fig.9 Output Wave Form for Proposed Full Adder

Fig.9 shows the Input and Output waveform of the proposed full adder is simulated.

Table 3 Comparison Table for Full Adder

Parameters	Conventional	IEEE (GDI)	Proposed (GDI)
No. of transistors used	28	10	6
Static power	2.91e-09	4.41e-09	1.97e-09
Dynamic power	2.56e-08	1.31e-08	4.24e-09
Delay	6.56e-09	6.34e-09	6.25e-08
PDP static	1.91e-17	2.80e-17	1.23e-17
PDP dynamic	1.68e-16	8.32e-17	2.64e-17

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Table 3 shows the comparison of Full adder using conventional MOS transistor, IEEE GDI, and Proposed GDI is listed of there. Proposed GDI uses less number of transistors to realize the Full adder operation. In the proposed method dynamic power consumption is reduced by 64% compared with conventional method.

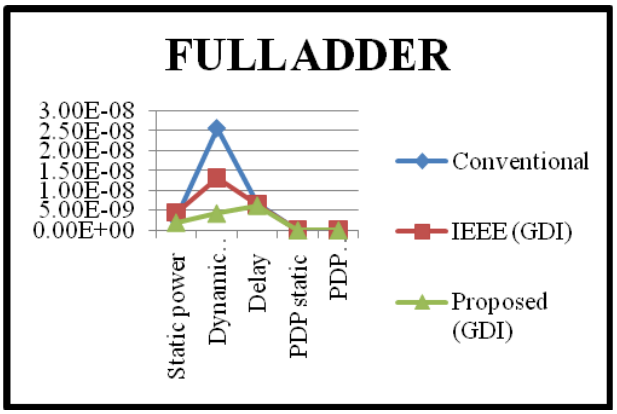

Fig.10 Comparison Chart for Full Adder

From these simulation results, the GDI based digital circuits are consumed less area, less power and less delay compared with conventional digital circuits.

From these simulation results, the GDI based digital circuits are consumed less area, less power and less delay compared with conventional digital circuits.

5. CONCLUSION

An effective Gate Diffusion Input (GDI) technique is used in the proposed circuits to reduce the area by reducing the number of transistors used. It is apparent from the power consumption, that the GDI technique provides better performance than conventional techniques. And also it reduces the dynamic power, static power, delay, static power delay product, dynamic power delay product.

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Krithiga Sukumaran She received her B.E degree in Electronics and Communication Engineering from Madras University and M.E degree in Applied Electronics from College of Engineering, Guindy. Currently working as a Assistant Professor in Thanthai Periyar Government Institute of Technology, Vellore since April 2013 and pursuing the research work in the field of Compressed Sensing for Image Processing Applications in Anna University, Chennai

Janani Munisamy She received her B.E degree in Electronics and communication Engineering from Thanthai Periyar Government Institute of technology,Vellore and M.E degree in Applied Electronics from College of Engineering,Guindy,India.She is currently working as Assistant Professor in Thanthai Periyar Government Institute of Technology, Vellore, India.Her field of interest includes VLSI Design and Consumer Electronics . She is currently pursuing her Ph.D in the field of VLSI Design.